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Search History

DATE: Wednesday, February 15, 2006 Printable Copy Create Case

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DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L28	L27 same design	9	L28
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L26	L1 and l2	8	L26
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L14	assign$ same pin same port	15454	L14
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L9	L8 same l3	25	L9
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L6	L1 same l3	129	L6
L5	L1 same l2	1	L5
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L3	display$	1946708	L3
L2	electronic adj1 image	11475	L2
L1	pin same port same test$	4744	L1

END OF SEARCH HISTORY

L28: Entry 1 of 9 File: USPT Mar 9, 2004

DOCUMENT-IDENTIFIER: US 6704910 B2
TITLE: Method for designing an integrated circuit containing multiple integrated circuit designs

Brief Summary Text (26):
The netlists for the individual designs are combined by a computer program into one multi-design netlist. The multi-design netlist includes a pin-pad assignment table that assigns numbered ports of each design to numbered I/O buffers, to numbered bonding pads, and to numbered package pins. The multi-design netlist includes, in addition to the netlists for the individual designs, provision for accessing the designs via shared bi-directional input/output buffers, and also includes logic for enabling only the outputs of one design at a time. EDA tools are then applied to the multi-design netlist to generate mask layouts. The mask layouts are used in a mask making facility to produce a mask set. The mask set is used to process silicon wafers. After fabrication is completed, the wafers are electrically probe tested. In this procedure, probes are placed on bonding pads on a die and each of the designs can be tested. The testing of all the designs on the die can be completed in one probing operation, each of the designs being operated in turn. The wafer is then cut into individual dice, each die containing the set of designs. Each die is then assembled into a semiconductor package with connections between bonding pads and package pins being made in accordance with the pin-pad assignment table. During assembly, access to the various designs in the multi-design integrated circuit can be restricted or can be left unrestricted. In either case, access to any design is made by applying appropriate signals to design active pins.

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L16: Entry 2 of 8 File: EPAB Apr 18, 2001

DOCUMENT-IDENTIFIER: EP 1092983 A1
TITLE: Integrated circuit tester with multi-port testing functionality

Abstract Text (1):
CHG DATE=20010503 STATUS=O> Disclosed is an automated test equipment - ATE - (200) having a tester-perpin architecture with a plurality of individual decentralized per-pin testing units (700), wherein each per-pin testing unit (700i) being adapted for testing a respective DUT-pin (di) of a device under test - DUT - (600) by emitting stimulus response signals to the respective DUT-pin and/or receiving stimulus response signals from the respective DUT-pin. For testing the DUT, the following steps are executed: defining - for a testing sequence - the DUT into one or more DUT-cores representing one or more functional units of the DUT and covering one or more DUT-pins of the DUT, and assigning - during the testing sequence - one or more of the per-pin testing units (700i) to one or more ATE-ports (210-240), whereby each ATE-port comprises one or more of the per-pin testing units (700i) and represents an independent functional testing unit for testing one or more of the DUT-cores during the testing sequence. <IMAGE>

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L12: Entry 3 of 8 File: USPT Apr 11, 2000

DOCUMENT-IDENTIFIER: US 6049896 A
** See image for Certificate of Correction **
TITLE: Method and system for indicating computer status

Detailed Description Text (13):
FIG. 3b illustrates the standard pin assignments for a parallel port 104 (FIG. 1) having a DB-25 female connector for coupling to the port connector 132 comprising a DB25 male connector. In a preferred embodiment, the system monitor 122 (FIG. 2) communicates signals indicating the burn-in status of the SUT 100 (FIG. 1) to the status indicator 126 using data pins of the parallel port 104 (FIG. 1). As shown in FIG. 3b, the data pins are the second through ninth pins of the parallel port (pins 2-9). Note also that the ground pins are the eighteenth through twenty fifth pins. In a preferred embodiment, the system monitor 122 (FIG. 2) may use any three distinct data pins, such as the third pin 140, the fourth pin 142 and the fifth pin 144, to communicate the signals indicative of the burn-in test status to the visual display elements 134, 136, 138.

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L28: Entry 2 of 9 File: USPT Dec 17, 2002

DOCUMENT-IDENTIFIER: US 6496058 B1
TITLE: Method for designing an integrated circuit containing multiple integrated circuit designs and an integrated circuit so designed

Brief Summary Text (26):
The netlists for the individual designs are combined by a computer program into one multi-design netlist. The multi-design netlist includes a pin-pad assignment table that assigns numbered ports of each design to numbered I/O buffers, to numbered bonding pads, and to numbered package pins. The multi-design netlist includes, in addition to the netlists for the individual designs, provision for accessing the designs via shared bi-directional input/output buffers, and also includes logic for enabling only the outputs of one design at a time. EDA tools are then applied to the multi-design netlist to generate mask layouts. The mask layouts are used in a mask making facility to produce a mask set. The mask set is used to process silicon wafers. After fabrication is completed, the wafers are electrically probe tested. In this procedure, probes are placed on bonding pads on a die and each of the designs can be tested. The testing of all the designs on the die can be completed in one probing operation, each of the designs being operated in turn. The wafer is then cut into individual dice, each die containing the set of designs. Each die is then assembled into a semiconductor package with connections between bonding pads and package pins being made in accordance with the pin-pad assignment table. During assembly, access to the various designs in the multi-design integrated circuit can be restricted or can be left unrestricted. In either case, access to any design is made by applying appropriate signals to design active pins.

L28: Entry 3 of 9 File: USPT Jun 11, 2002

DOCUMENT-IDENTIFIER: US 6405355 B1
TITLE: Method for placement-based scan-in and scan-out ports selection

Detailed Description Text (40):
In order to conserve chip device pins, designers sometimes use functional pins for scan-in and scan-out ports of the scan chain. Typically, functional pins are assigned as scan-in and scan-out ports by a DFT (Design For Test) tool during the scan insertion process (e.g., process 120) based on schematic information. This approach, however, is not ideal because the designations of particular functional pins as being scan-in and scan-out ports may restrict the layout processes from placing scan cells in the best possible positions. In addition, if inappropriate scan-in and scan-out ports are selected before cell placement, scan cells may be placed in positions that require an excessive amount of routing resources for connecting the scan cells to the scan-in and scan-out ports. As a result, place-and-route processes may be hindered from fully optimizing the layout of the integrated circuit design.

US 20050071715A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2005/0071715 A1

Kolman (43) Pub. Date: Mar. 31, 2005

(54) METHOD AND SYSTEM FOR GRAPHICAL PIN ASSIGNMENT AND/OR VERIFICATION

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(51) Int. Cl.[7] G01R 31/28

(52) U.S. Cl. 714/724

(57) ABSTRACT

A method, a system and/or a computer readable medium for accessing design data including an electronic image of an integrated circuit to be tested; determining whether a pin of the integrated circuit has been assigned to a port in a multi-port automated test environment; enabling a displayable pin indicator based in part upon the determination of whether a pin is assigned to a port; and displaying the electronic image and the displayable pin indicator.